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Measurement of process-induced defects in Si sub-micron devices by combination of EDMR and TEM

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Abstract. Process-induced defects are a serious issue for modern sub-micron Si LSIs. To characterize such defects, two different techniques are useful: electrically detected magnetic resonance (EDMR) and transmission electron microscope (TEM), which can detect small (point) and extended defects, respectively. We applied EDMR and TEM to the issue of defect-induced leakage currents in dynamic-random-access memory (DRAM) cells. For our DRAM samples (a 0.25-μm-rule series), although TEM showed no extended defects, EDMR successfully detected two types of point defects: V_2+O_x (Si divacancy-oxygen complexes) and larger Si vacancies (at least larger than V_6). We confirmed that these defects are the source of DRAM leakage currents. The observed defects were formed by ion implantation processes, but were more thermally stable than those in bulk Si crystals. The origins of this enhanced stability are attributed to the presence of oxygen atoms and a strong mechanical strain in LSIs. To clarify the origin of the complicated strain in LSI structures, we can directly measure the local-strain distribution in DRAM samples by means of convergent-beam electron diffraction (CBED) using TEM, which provides us with a valuable hint for understanding the formation mechanism of process-induced defects.

PACS. 85.40.-e Microelectronics: LSI, VLSI, ULSI; integrated circuit fabrication technology – 85.30.De Semiconductor-device characterization, design, and modeling – 61.72.-y Defects and impurities in crystals; microstructure

1 Introduction

Process-induced defects are quite important for deep sub-micron Si large-scale integrated circuits (Si LSIs). In modern Si LSIs, more than millions components (such as transistors) are fabricated in a chip. To ensure this chip works correctly, the fraction of defective components must be smaller than 10^{-6} components/chip. This implies that even a small number of defects potentially cause a serious failure and/or reliability degradation of Si chips. Moreover, process technologies employed tend to become more complicated with the progress of LSIs, which are likely to result in the formation of more process-induced defects. Therefore, recognition of defects becomes increasingly important for LSI technologies. However, it is generally difficult to obtain information about such defects, because a conventional spectroscopy can not access to the inside of small Si LSIs.

To characterize process-induced defects, we used two different techniques: electrically detected magnetic resonance (EDMR) and transmission electron microscope (TEM). Since EDMR detects electron-paramagnetic-resonance (EPR) signals via device currents, this technique is applicable to LSIs and is able to identify point defects that contribute directly to the device current [1–3]. EDMR seems to be a promising probe for small defects, because EPR has greatly improved our understanding for point defects in bulk Si crystals. TEM, on the other hand, is of course useful for structural identification of defects with larger dimensions than point defects [4]. Furthermore, this tool is also capable of probing local strain through convergent-beam electron diffraction (CBED) analysis [5–7]. Using CBED, we can directly measure a local-strain distribution in actual devices, which gives us a valuable hint to understand the formation scenario within device structures.

In this paper, we present an interesting example studying process-induced defects in dynamic-random-access memory (DRAM) cells (Figure 1). In this type of device, leakage currents of a memory cell must be minimized to maintain the charge retention time as long as possible (Figure 1(b)). However, if process-induced defects were formed in the $n^+ - p$ junction connected to a capacitor, they increase the leakage current (Figure 1(c)), resulting in a serious degradation of the retention time [8]. We first tried to observe defects by TEM, but no detectable defects were found, although the leakage current level suggested the presence of defects. This result indicated that smaller

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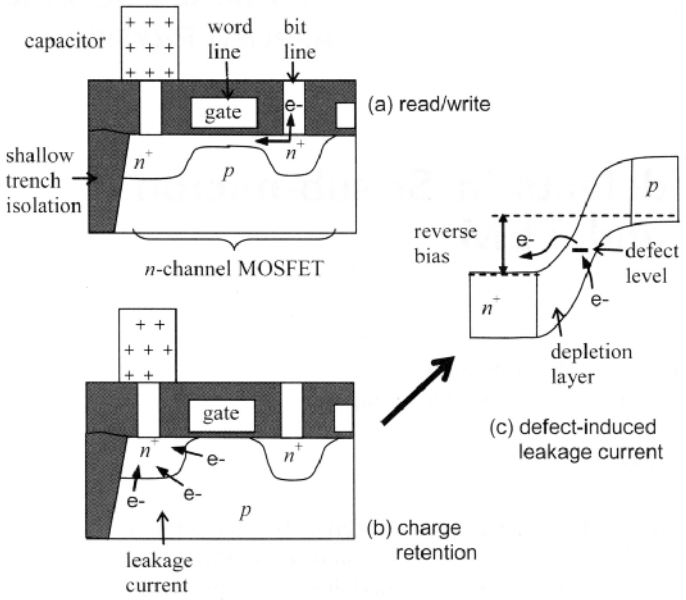

Fig. 1. Issue of DRAM leakage currents. (a) DRAM cell in a read/write operation. (b) Charge retention operation. Leakage currents in the $n^+ - p$ junction reduce the capacitor's charges. (c) Band diagram for defect-induced leakage currents.

defects are related to this issue, and we therefore applied EDMR. Then, it was successfully found that the leakage current is generated through two types of defects, and that their atomic structures are based on Si vacancies. In the next step, we investigated how they were formed in the device. Our finding is that the formation of these defects is related to a strong lattice strain in the LSI structures. We finally show that the origin of such a built-in strain can be assessed by our high-resolution CBED analysis.

2 EDMR study on Si LSIs

2.1 EDMR method

The principle of EDMR is simply described in Figure 2. If

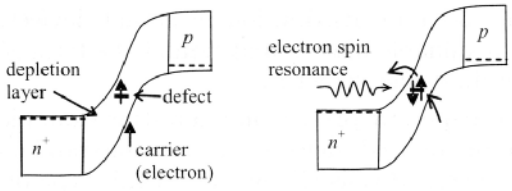

Fig. 2. The principle of EDMR. Assume a pair of a carrier (electron) and a spin-1/2 defect. Under a magnetic field, both electrons prefer to have a spin of the same direction. For this spin-parallel configuration, the carrier can not access to the defect level. If the spin of the defect is excited to the opposite direction, then the current path via this defect is open and the sample current is changed. EDMR monitors this current change.

a defect level in the energy gap has an unpaired electron (an electron spin, $S = 1/2$), the carrier transport process via this defect is possibly spin dependent. In such a case, the sample current will be changed when electron spin resonance takes place at this defect. EDMR monitors this resonant current change, and the spectrum obtained is basically equivalent to that of EPR. In contrast with EPR, sensitivity of EDMR does not depend on the sample volume but on sample current, and hence this technique is quite suitable for a small volume of Si LSIs.

In n- or p-type regions of a device, a defect level generally loses an unpaired electron, due to the formation of doubly-occupied or empty states, respectively. Therefore, EDMR is usually sensitive to the defects in the depletion layer of a device. The depletion layer width depends strongly on the bias condition and it is necessary for signal detection to adjust the depletion layer to cover the defects. This point will be discussed in more detail in the following section.

For taking EDMR spectra with optimal signal-to-noise ratio, it is also essential to select what sort of device current is used for EDMR. In principle, the signal intensity (normalized current change, $\Delta I/I$) is determined by the fraction of defect-induced currents in a total current. For the case of p-n junctions, previous studies were often performed under a forward bias or photo illumination to excite a large junction current. In these conditions, however, the sample current was dominated by diffusion currents which are independent of defects. Therefore, EDMR signals were usually very small, for example $\Delta I/I = 10^{-6}$ to 10^{-5} [1,2], which made it difficult to identify the origin of signals. For this reason, the creation of additional defects by electron or γ-ray radiation damages was often carried out in previous studies [1,9]. On the other hand, leakage currents in a reverse-biased p-n junction (junction leakage currents) are generally dominated by defect-induced currents (generation current). We found that EDMR using these leakage currents are much more sensitive to defects rather than using forward-biased or photo-excited currents [3]. Our EDMR measurements on Si LSIs were carried out using such leakage currents, which was the key to observe process-induced defects in device-quality samples without any intentional damages. The same situation may also hold for leakage currents in dielectric layers, if the direct leak is lower than the defect-assisted leak. In fact, EDMR was used to study gate insulators of Si LSIs and revealed defects in very thin (nm-order in thickness) layers [10,11]. These are other interesting applications of EDMR to Si LSIs.

The detection limit of EDMR has not been clearly assessed yet, although it has been generally accepted that EDMR has a sensitivity at least several orders of magnitude higher than conventional EPR. We have examined the smallest Si device which is enough for detecting EDMR signals. The signal detection was possible at least for an array consisting of 10 metal-oxide-semiconductor field-effect transistors (MOSFETs), as shown in Figure 3. Thus, we expect that even a single MOSFET within a LSI may be sufficient for EDMR studies.

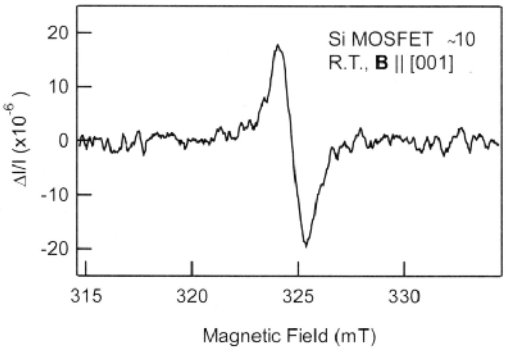

Fig. 3. EDMR spectrum measured for an array consisting of ten Si MOSFETs (n-channel, gate length = 0.25 μm, gate width = 0.5 μm). The current monitored was driven from the drain to the source by a bias of 1 V and a gate voltage of −3.5 V. Acquisition time was 4 minutes. This signal is the same as signal B described in the section 2.2.

2.2 Example: DRAM leakage currents

Actually, we have applied EDMR to the leakage currents of DRAM cells, to study the microscopic origins of these currents [3]. This section describes how EDMR was applied to Si LSIs, following this example.

Our LSI samples were fabricated by a 0.25 μm-rule DRAM process. We cut 0.5×0.5 cm^2 chips from the wafer, then mounted them on sample tubes and made electrical contacts to them. These chips (test element groups) included an array of 54000 DRAM cells (n-channel MOSFETs) without capacitors (Figure 4(a)). We measured EDMR for a total leakage current flowing from the source

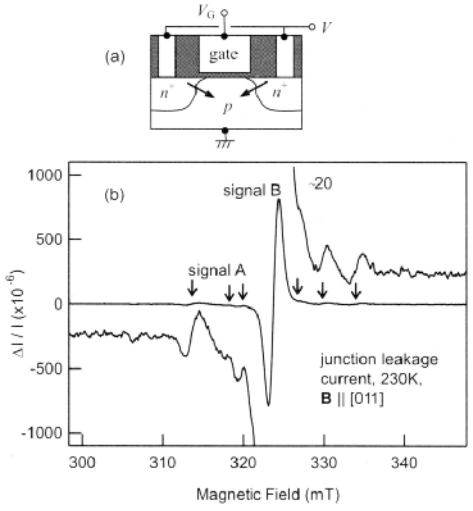

Fig. 4. EDMR measurement on DRAM leakage currents. (a) Samples we used were n-channel MOSFETs of DRAM cells without capacitors. (b) EDMR spectra measured for V = 7.3 V, V_G = −4.5 V, microwave power of 200 mW, and magnetic-field modulation with 0.4 mT at 320 Hz.

and drain (n^+-type layer) to the p-type substrate by applying a reverse voltage of 7.3 V. These measurements were carried out at 230 K to maximize the signal-to-noise ratio and maintain normal current-voltage characteristics. Further details of our experiments have been published in our previous reports [2,3].

Figure 4(b) shows a typical EDMR spectrum for the DRAM leakage current. Note that the $\Delta I/I$ value is of the order of 10^{-4}, which is much higher than the typical value (10^{-6}) under forward-biased conditions [2]. In this spectrum, two signals are clearly observed, which we call signal A and B in this paper.

Figure 5(a) shows the angular dependence of signal A when rotating the magnetic field (**B**) in the Si $(0\bar{1}1)$ plane.

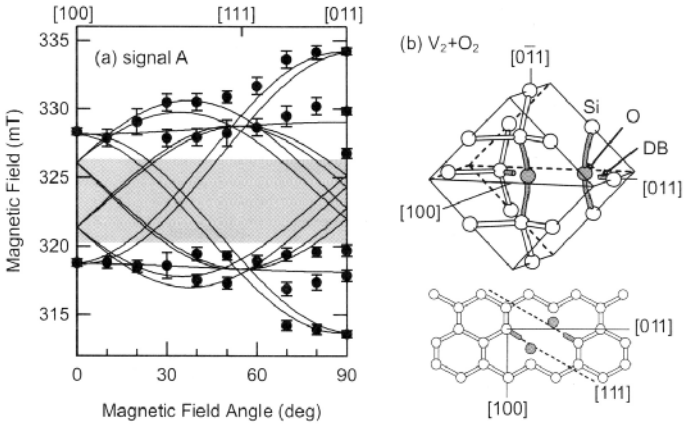

Fig. 5. Analysis of signal A. (a) Angular dependence of signal A for the **B** rotation in the $(0\bar{1}1)$ plane. In the gray area, signal A was not clear due to overlapping of signal B. Solid lines are calculated by adopting the defect system of V_2+O and V_2+O_2. (b) Origin of signal A (V_2+O and V_2+O_2).

This pattern was found to fit well to the fine splitting that is caused by a pair of Si dangling bonds (DBs) aligned to ⟨111⟩ axes. The solid lines in the figure were calculated by assuming a defect system of such a DB pair, which seems to agree well with experimental data. Previously, it was reported in radiation-damaged bulk Si crystals that DB pairs are formed in vacancy-oxygen complexes [12–15]. For these DB pairs, the fine-splitting width is determined by the R^{-3} dependence (R = separation between DBs) or the number of Si vacancies, as shown in Figure 6. Obviously, the fine interaction of signal A is in good agreement with those obtained for the V_2+O (the A14 center) or V_2+O_2 (the P2 center) [12,13]. Thus, we have concluded that signal A originates from a combination of the A14 and P2 spectra. The A14 and P2 centers have a common atomic structure, as shown in Figure 5(b).

On the other hand, signal B was similar to the well-known Si DB signal (g = 2.0055, isotropic) observed in amorphous Si [16] or damaged Si crystals [2,9,17,18], however, this signal is in fact anisotropic unlike the g = 2.0055 signal (Figure 7(a)). This anisotropy clearly indicates that the Si DBs are not randomly oriented in our samples. Furthermore, we can exclude the possibility of isolated DBs, because their spectra are characterized by split lines, as observed in the P_{b0} spectrum [2]. Therefore, we con-

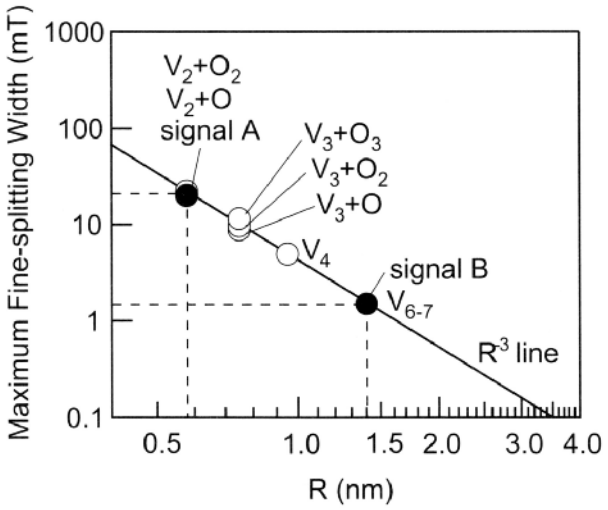

Fig. 6. Maximum fine-splitting width versus DB-DB distance (R) for various vacancy-oxygen complexes (open circles) [12–15] and EDMR signals (solid circles).

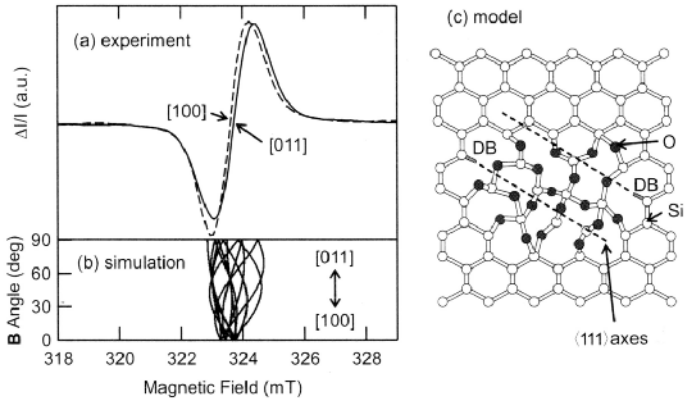

Fig. 7. Analysis of signal B. (a) Experimental spectra of signal B measured for the two **B** directions. (b) Simulated angular dependence of signal B by assuming the model of a DB pair ($R = 1.5$ nm) shown in (c). (c) Atomic model for the origin of signal B.

sider that the observed DBs interact with each other only weakly (i.e., R is large), so that the split lines are smeared out by weak fine interactions. An analogy with signal A indicates that such DB pairs are likely involved in Si vacancies. Look again at Figure 6. For signal B, the maximum fine-splitting width should be less than the full width at half maximum (FWHM) of this signal (= 1.5 mT). From this figure, we have estimated that R should be larger than 1.4 nm or the vacancy size is at least larger than V_6. We have also confirmed that the angular dependence of Si DB pairs of R larger than 1.4 nm approximately reproduces the experimental spectra (Figure 7(b)). Since the fine splitting is weak and complicated, a complete signal forms a single broad peak for any rotation angle, as observed experimentally. Accordingly, we propose that signal B arises from a series of large Si vacancies (at least larger than V_6), which leave weakly interacting Si DBs ($R \geq 1.4$ nm). These large vacancies are very likely to accommodate oxygen atom(s) during high-temperature processes, similarly to the origin of signal A. Figure 7(c) illustrates our model for the origin of signal B. We suggest that they are the small type of the oxide precipitates observed by TEM on Czochralski Si wafers [19].

The EDMR signals of A and B were only detectable when the gate of MOSFETs was negatively biased. Under this condition, the depletion layer expands into the near-surface region of the source and drain (n^+-type region), as shown in Figures 8(a) to (b). Therefore, it is concluded

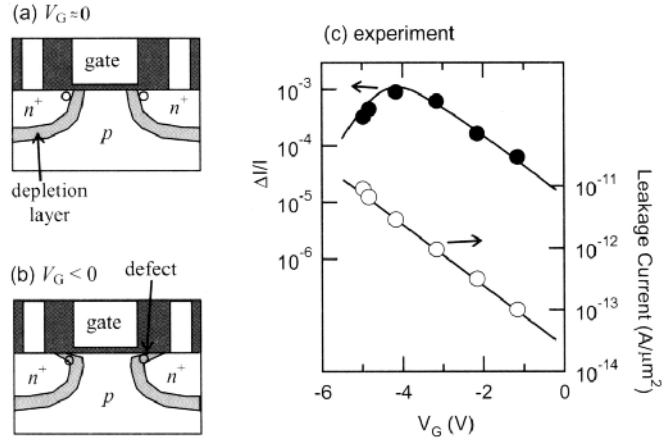

Fig. 8. Effect of gate bias. The near-surface depletion layer is changed by the gate bias (V_G) as shown in (a) and (b). (c) V_G-dependence of the leakage current and $\Delta I/I$. The $\Delta I/I$ value was measured for a peak height at 324.4 mT.

that the observed defects were distributed in the near-surface n^+-type region in the vicinity of the gate. If we increased the negative gate voltage, the EDMR signal intensity exponentially increased together with the leakage current (Figure 8(c)). This good correlation ensures that the source of the leakage current is the observed defects. It should be noted that the observed increase in the leakage current is known as gate-induced drain leakage (GIDL) [8, 20], which is an important issue for not only DRAMs but also logic LSIs. Thus, we also concluded that the GIDL phenomenon is related to the present defects. As the gate bias increased further, the leakage current continued to increase but the $\Delta I/I$ decreased. This implies that direct tunneling of carriers through the depletion layer started to occur.

2.3 Formation mechanism of Si vacancy-type defects

Judging from the microscopic structure (Si vacancy-type) and location (n^+-type region) of the defects, it is reasonable to conclude that they were created by phosphorous implantation in the n^+-type region. We would like to emphasize that even our low-dose implantation ($\approx 10^{13}$ cm^{-2}), which did not create any detectable defects in TEM analyses, caused such defect formation. In our samples, signal B (large vacancies) was always much stronger than signal A (V_2+O and V_2+O_2). This is quite

reasonable, because the larger vacancies tend to show higher thermal stability, as observed in radiation-damaged Si [12]. After implantation, however, our chips were subjected to annealing at a temperature higher than 800 °C, which is much higher than the reported anneal-out temperature (< 400 °C) for V_2+O and V_2+O_2 in bulk Si [12]. In addition, the $g = 2.0055$ signals usually disappear when implantation-damaged Si wafers are annealed in the relevant temperature range [18]. Therefore, the Si vacancy-type defects appeared to be thermally more stable in LSI structures than in bulk crystals.

We attribute such an enhanced thermal stability to two factors. The first one is the strong compressive strain in Si LSIs. It has been experimentally revealed that the compressive strain increases monotonically with narrowing MOSFET width (W), and it is over 500 MPa when W is in the sub-micron range [5,21,22]. Generally, under such a compressive strain, Si vacancies become thermally stable, because they can relax the compressive strain of the Si-Si bonds [23]. Although this energy gain (= pressure coefficient of the vacancy formation energy, ΔE_f) has not been determined for the vacancy-oxygen complexes, the simplest case of a Si monovacancy (V_1) reveals that $\Delta E_f = -0.1$ eV at a compressive stress of 600 MPa.Even with this small ΔE_f, V_1 will be about 3 times [$\approx \exp(\Delta E_f / k_B T)$, where k_B is the Boltzmann constant] more stable at $T = 800$ °C and 600 MPa, as compared to a zero-stress situation. It is thus quite possible that more Si monovacancies can remain in a MOSFET with smaller dimensions, yielding more Si vacancy defects. To confirm the strain effect, we carried out EDMR measurements on a series of DRAM samples which have three different W (24, 2.4, and 0.8 μm). Then, comparing EDMR signal intensities for these samples, it was found that the EDMR intensity increased significantly with narrowing W (Figure 9). This result supports that a larger number of defects is created in more strained MOSFET region.

The second important factor is the oxygen incorporation into a specific device region. It was already known that Si vacancies become increasingly stable when they couple with more oxygen atoms [12]. Although our devices were fabricated in a high-purity epitaxially-grown Si layer, oxygen incorporation may occur in near-surface regions during surface oxidation and dopant implantation through scattering oxides. We thus expect that Si vacancy-type defects tend to remain in such regions, as observed experimentally. Recently, a similar phenomenon was found by positron-annihilation measurements on SIMOX (separation by implanted oxygen) Si wafers [24]. For this case, vacancy-oxygen complexes were detected in the near-surface regions that contain two-orders of magnitude higher concentration of oxygen atoms (10^{20} cm^{-3}) than a typical value for conventional Si wafers. These complexes were stable even in 1300 °C processes. Interestingly, their sizes were tentatively estimated to be V_1 to V_2 or larger than V_6, which is quite consistent with our microscopic data.

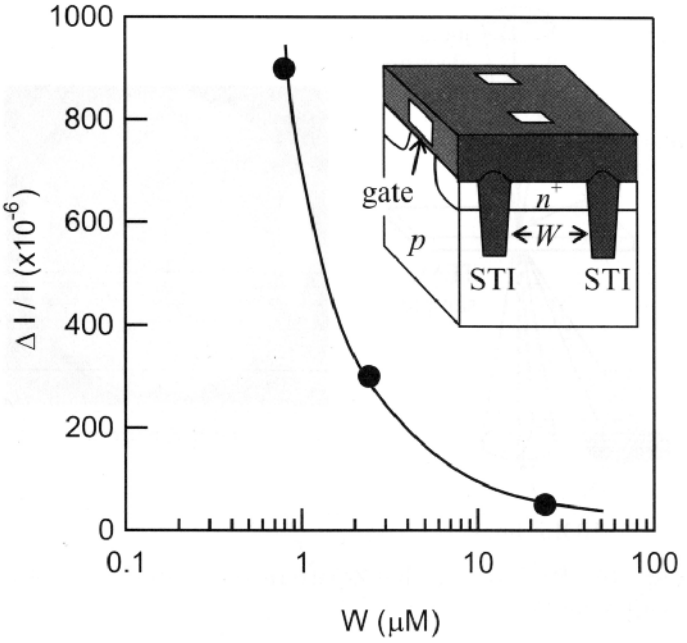

Fig. 9. Influence of the MOSFET width (W) on EDMR signal intensity ($\Delta I/I$). Narrowing W causes more defect formation (higher $\Delta I/I$) in this region. The $\Delta I/I$ value was measured with $V = 7.3$ V and $V_G = -4$ V.

3 TEM (CBED) study on Si LSIs

As was seen above, a strong local strain inside LSIs correlates with increased probability for defect formation. It is widely accepted that a major source of the strain is device isolations (in modern LSIs, shallow trench isolations (STIs) are mostly used) which introduce a strong compressive strain in the active regions [5,7,21,22]. However, other structural features such as gate electrodes (poly-Si), sidewall layers (SiN_x), contact plugs (poly-Si, metal silicides) would also generate the strain, so that in general, actual strain distribution becomes very complicated. Therefore, a tool for directly measuring local-strain distribution in actual devices is strongly required in modern LSI technologies. For this purpose, CBED measurements using a TEM system has great advantages of a high special resolution ($\sim$ 10 nm) and a high sensitivity ($\sim 2 \times 10^{-4}$ of lattice-constant change). We thus performed CBED measurements on DRAM samples to determine the actual strain distribution in this type of device.

The principle of CBED is illustrated in Figure 10 [5–7]. Using a focused electron probe, we can obtain an electron diffraction pattern from a desired position in a TEM sample, which is composed of a number of higher-order Laue zone (HOLZ) lines (the picture in Figure 10). The positions of these HOLZ lines are shifted by the change of diffraction condition due to strain. By fitting the HOLZ lines between observation and kinematical calculation, a local strain is determined.

In our CBED experiment, TEM samples were first prepared by focused ion beam (FIB) technique. Figure11(a) is a schematic of our DRAM cells examined. Then, we measured CBED at 12 points shown in the figure, and then de-

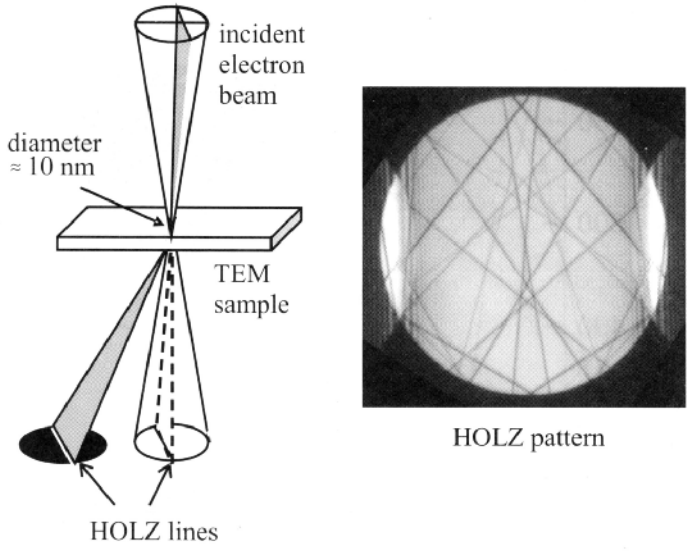

Fig. 10. Principle of HOLZ-pattern observation in CBED measurements.

termined each local strain value by computer simulations of HOLZ patterns. The result is shown in Figure 11(b). As is consistent with previous works [5,7,21,22], a compressive strain is generated along the x direction due to STIs in our samples. On the other hand, in the edge of the gate electrode (point 8) or just beneath the contact plug (point 11), the local strain rapidly increased towards a tensile direction up to 6×10^{-4}, which is as large as the maximum compressive strain due to STIs. Thus, it is concluded that not only STIs but also other device structures significantly influence the strain generation.

In some special positions in LSI structures (e.g., points 3, 7, 8, and 11 in Figure 11), it is likely that the local strain is concentrated in a small volume. A similar phenomenon was observed in the case of LOCOS (local oxidation of Si) isolated devices [6]. We have confirmed that the strain induces dislocations at such highly-strained points [7]. Although we did not observe any dislocations in the present case, smaller defects were alternatively found in a Si lattice near the edge of the gate. Therefore, it is quite important for reducing process-induced defects to minimize the local strain maxima in LSI structures.

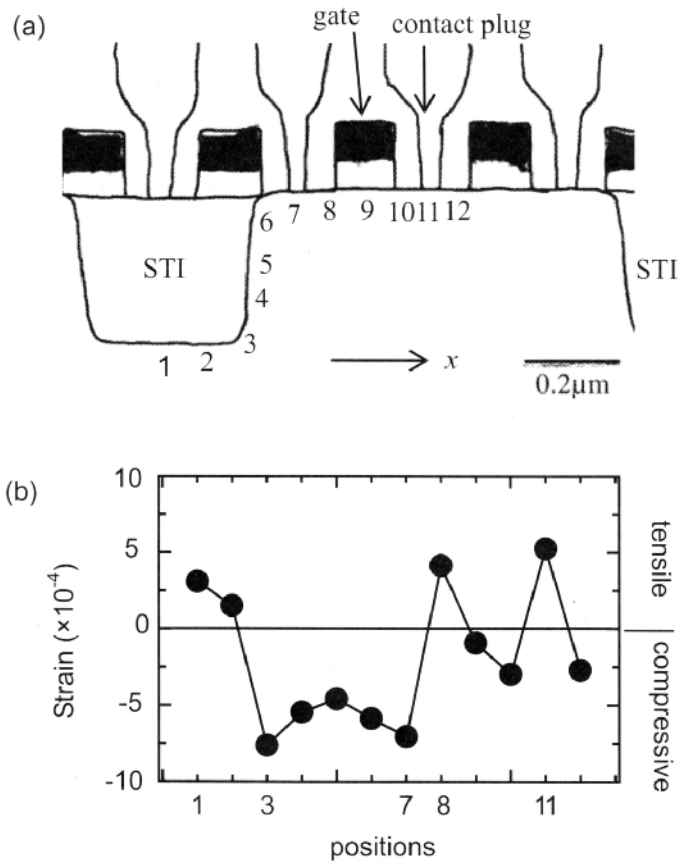

Fig. 11. CBED measurements on local strain inside a DRAM sample. (a) Sample structure determined by the TEM image. CBED measurements were carried out at 12 positions. (b) Local strain along the x direction determined by CBED.

4 Summary

To characterize process-induced defects located inside Si LSIs, we performed two different measurements using EDMR and TEM, which were useful for detecting small and large defects, respectively. In this paper, the capabilities of these two techniques was demonstrated by applying these to the well-known issue of defect-induced leakage currents in DRAM cells. Although TEM images showed no large defects on our DRAM cells, EDMR successfully revealed the presence of point defects in these samples, and demonstrated a good correlation between the defects and leakage currents. The defects observed by EDMR were two-types of Si vacancy-type defects (V_2+O_x and larger than V_6) which had been formed by ion-implantation process. We found that they become more thermally stable in LSIs than in bulk Si crystals. One origin of this enhanced stability was attributed to a strong lattice strain in LSIs, and thus it was important for understanding the formation mechanism of defects to clarify the source of the local strain. For this purpose, we performed CBED analyses, which were able to reveal a local-strain map of actual devices with a 10-nm resolution. Then, it was found that not only shallow trench isolations but also gate electrodes and contact plugs generate a strong local strain. At the local-strain maxima, extended defects such as dislocations were frequently introduced. Even if not, smaller defects would be alternatively formed, as suggested by our EDMR measurements. Therefore, to minimize the density of process-induced defects, it is important to minimize the strain by optimizing materials and processes of LSIs.

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